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DOCKET NO.: E0295.70126US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Stephen L. Scaringella et al.
Serial No:	09/364,727
Confirmation. No.:	9805
Filed:	July 30, 1999
For:	COMPUTER STORAGE SYSTEM INCORPORATING ON-BOARD EEPROMS CONTAINING PRODUCT DATA
Examiner:	Vo, Tim T
Art Unit:	2189

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

The undersigned hereby certifies that this document is being placed in the United States mail with first-class postage attached, addressed to Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the 22nd day of December, 2003.

Doris Ann Champagne

Doris Ann Champagne

Mail Stop Appeal Brief - Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith are the following documents:

[X] Appellants' Brief under 37 C.F.R. §1.192 (in triplicate)
[X] Return Receipt Postcard

The Notice of Appeal was date stamped by the PTO on October 20, 2003. Since December 20, 2003 falls on a Saturday, this Appeal Brief is timely filed.

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned at (617) 720-3500, Boston, Massachusetts.

A check in the amount of $330.00 is enclosed for filing an appeal brief. If the amount is insufficient, the balance may be charged to Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

Respectfully submitted,
Stephen L. Scaringella et al., Applicant

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Attorney's Docket No.: E0295.70126US00

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Mail-Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANTS' BRIEF UNDER 37 C.F.R. §1.192

Sir:

This brief is in furtherance of the Notice of Appeal mailed in this application on October 16, 2003 and date stamped by the Patent and Trademark Office on October 20, 2003. This brief is being filed in triplicate (37 C.F.R. §1.192(a)). This brief contains the following items under the headings and in the order set forth below (37 C.F.R. §1.192(c)).

I. REAL PARTY IN INTEREST (37 C.F.R. §1.192(c)(1))

II. RELATED APPEALS AND INTERFERENCES (37 C.F.R. §1.192(c)(2))

III. STATUS OF CLAIMS (37 C.F.R. §1.192(c)(3))

IV. STATUS OF AMENDMENTS (37 C.F.R. §1.192(c)(4))

V. SUMMARY OF INVENTION (37 C.F.R. §1.192(c)(5))

VI. ISSUES (37 C.F.R. §1.192(c)(6))

VII. GROUPING OF CLAIMS (37 C.F.R. §1.192(c)(7))

VIII. ARGUMENT (37 C.F.R. §1.192(c)(8))

IX. APPENDIX CONTAINING CLAIMS INVOLVED IN THE APPEAL (37 C.F.R. §1.192(c)(9))

I. REAL PARTY IN INTEREST (37 C.F.R. §1.192(c)(1))

The real party in interest in this application is the assignee, EMC Corporation, a corporation having a place of business at 171 South Street, Hopkinton, Massachusetts 01748-9103.

II. RELATED APPEALS AND INTERFERENCES (37 C.F.R. §1.192(c)(2))

There are no other appeals or interferences known to the Appellants, the Appellants' legal representative, or the assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS (37 C.F.R. §1.192(c)(3))

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application: 14

B. STATUS OF ALL THE CLAIMS

1.	Claims cancelled:	None
2.	Claims withdrawn from consideration but not cancelled	None
3.	Claims pending:	1-14

4. Claims allowed: None

5. Claims rejected: 1-14

C. CLAIMS ON APPEAL

The claims on appeal are claims 1-14.

IV. STATUS OF AMENDMENTS ((37 C.F.R. §1.192(c)(4))

No amendment was filed subsequent to the final rejection mailed on April 16, 2003. In response to the final rejection, Appellants filed a Request for Reconsideration, which was mailed on July 16, 2003. The Request for Reconsideration contained no claim amendments. In an Advisory Action mailed July 25, 2003, the Examiner indicated that the Request for Reconsideration did not place the application in condition for allowance.

V. SUMMARY OF INVENTION (37 C.F.R. §1.192(c)(5))

The present invention relates to methods and apparatus for identifying circuit boards in systems which include a plurality of circuit boards and a backplane for mounting and interconnecting the circuit boards. The invention is described in the context of a computer storage system, as shown in Figs. 1 and 2 of the present application. Fig. 1 is a block diagram of a computer storage system, and Fig. 2 is a simplified block diagram representative of each front end and back end director shown in Fig. 1. The computer storage system is described generally at page 3, line 29 to page 5, line 18.

The storage system includes one or more front end directors 20, 22, ...24, which are responsible for managing and translating read/write requests from a host computer 10 into one or more requests to the physical disk drives in the storage system. The front end directors are connected via buses 30 and 32 to a system cache memory. The system cache memory is coupled to disk drives 50, 52, ...54, through a back end director 60. The storage system may include one or more back end directors, each connected to one or more disk drives (Page 4, lines 2-16). The system of Fig. 1 includes back end directors 60, 62, ...64.

The system may be implemented as a plurality of printed circuit boards mounted in a backplane. Each director may be packaged as a printed circuit board. The backplane provides

interconnections between the directors, the system cache memory, the host computer and the disk array (Page 9, lines 13-16).

The same architecture may be used for front end directors 20, 22, ...24 and back end directors 60, 62, ...64. As shown in Fig. 2, the director includes data movers 110 and 112 which are controlled by X processor 120 and Y processor 122, respectively (Page 4, line 27 to Page 5, line 10). Each director also includes shared resources 140 (Page 5, lines 11-18).

Each director may include a non-volatile memory in the form of a serial, electrically-erasable, programmable, read-only memory (EEPROM) 150 which is part of the shared resources of the director. The non-volatile memory stores product data that uniquely identifies the director board. Product data stored in the serial EEPROM 150 may include a board part number, a board serial number, a board revision level, a cabinet serial number and text comments (Page 17, lines 1-8). The product data may be read from serial EEPROM 150 by processors 120 and 122 and may be accessed externally for testing and other purposes. The on-board serial EEPROM 150 is advantageous because product data is stored with the product itself rather than in a host computer or other storage location (page 17, lines 10-13).

VI. ISSUES (37 C.F.R. §1.192(c)())

A. Whether each of claims 1-4, 6 and 12-14 is unpatentable under 35 U.S.C. §103(a) over Dorfman, et al., U.S. Patent No. 6,118,862 (hereinafter Dorfman) in view of Don, et al., U.S. Patent No. 6,266,740 (hereinafter Don).

B. Whether each of claims 5 and 10 is unpatentable under 35 U.S.C. §103(a) as unpatentable over Dorfman in view of Don and further in view of Wilhelm, U.S. Patent No. 5,761,033 (hereinafter Wilhelm).

VII. GROUPING OF CLAIMS (37 C.F.R. §1.192(c)(7))

A. Group I. For purposes of this appeal only and for the rejection under 35 U.S.C. § 103(a), claims 1-4 and 6 stand or fall together. Claim 1 is representative.

B. Group II. For purposes of this appeal only and for the rejection under 35 U.S.C. § 103(a), claim 5 stands or falls alone.

C. Group III. For purposes of this appeal only and for the rejection under 35 U.S.C. § 103(a), claims 7-9 and 11 stand or fall together. Claim 7 is representative.

D. Group IV. For purposes of this appeal only and for the rejection under 35 U.S.C. § 103(a), claim 10 stands or falls alone.

E. Group V. For purposes of this appeal only and for the rejection under 35 U.S.C. § 103(a), claims 12-14 stand or fall together. Claim 12 is representative.

VIII. ARGUMENT ((37 C.F.R. §1.192(c)(8))

A. The rejection of claims 1-4, 6, 7-9, 11 and 12-14 under 35 U.S.C. § 103(a) as unpatentable over Dorfman in view of Don should be reversed. The claims of groups I, III, and V have been finally rejected under 35 U.S.C. §103(a) as unpatentable over Dorfman in view of Don. Each of the claim groups is addressed individually below.

The Dorfman patent discloses a computer telephony server for simultaneously implementing a plurality of messaging applications. The server includes a processor, a memory and a plurality of slots connected to the processor through a high speed bus, each of the plurality of slots being adapted to receive an interface card for connecting the sever to an external resource (Abstract). As shown in Fig, 2 of Dorfman, the computer telephony server 10 includes a processor board 50 and a backplane 60. The processor board 50 includes a processor 52, a memory 54 and a disk controller 56 which is coupled to a hard drive 58. The backplane 60 includes a plurality of slots 62a-62f which are connected to a bus. (Column 4, lines 13-31).

The Don patent discloses a method for verifying the organization of a magnetic disk storage system in which individual storage logical volumes are grouped in sequences as components of a meta device. (Abstract). The disk storage system includes multiple disk drives (Column 1, lines 16-23). In some applications, the required capacity for a storage logical volume exceeds the capacity of a physical drive. In this case, a number of storage logical volumes are concatenated into a predetermined sequence as a meta device wherein each storage logical volume is a meta member. A meta device acts as a single host logical volume that a host addresses. With this approach, a host logical volume size becomes independent of physical drive capacity (Column 1, lines 36-50).

A problem associated with the meta device is that the physical disk drives may be exchanged, resulting in data loss (Column 1, lines 51-63). To overcome this problem, the Don patent describes a method wherein each storage component or meta member of a meta device

has a unique signature. A dedicated storage area in each disk drive has a predetermined value in a signature field. The unique signature comprises certain configuration data for the storage logical volume. A separate configuration file stores configuration data for each component. During an integrity analysis, the signature in the dedicated storage area and the configuration data common to the dedicated storage area and the configuration file are analyzed to confirm that the storage logical volume possesses all characteristics corresponding to those in the configuration file (Column 2, lines 1-39).

1. The claims of Group I patentably distinguish over Dorfman in view of Don.

For the claims of Group I, claim 1 is representative. Claim 1 is directed to apparatus comprising a plurality of circuit boards, each having electronic circuitry including a non-volatile memory containing product data that identifies the respective circuit board and means for reading the product data in the non-volatile memory, and a backplane for mounting and interconnecting the circuit boards.

The Examiner asserts that Dorfman discloses a plurality of circuit boards and a backplane for mounting and interconnecting the circuit boards, but acknowledges that Dorfman does not teach circuit boards including a non-volatile memory containing product data that identifies the respective circuit board and means for reading the product data in the non-volatile memory, as required by claim 1. The Examiner relies upon Don for teaching a memory for storing ID data such as cabinet serial number, device number, etc.

As a basis for the combination of Dorfman and Don, the Examiner relies upon a statement in Dorfman that "other hardware configurations could be utilized." Based on this suggestion, the Examiner asserts that Don provides "a local memory for storing ID data (ID codes) such as cabinet serial number, device number (column 5, line 54). Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention to modify Dorfman's invention to include product data on the memory that is included on the processor boards in order for each board to have its own unique identification means" (Office Action page 6, paragraph 5). The cited portion of Dorfman states that other hardware configurations could be utilized. Dorfman further states that the preferred embodiment is a passive backplane

but that the computer telephony server could be implemented with an active backplane (see column 4, lines 55-65 of Dorfman).

It is respectfully submitted that the Examiner has not established a *prima facia* case of obviousness based on the alleged combination of Dorfman and Don. One of the three basic criteria for a *prima facia* case of obviousness is that there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings (MPEP §2143). It is submitted that the Examiner has failed to establish a suggestion or a motivation to combine the reference teachings. It is true that backplanes containing printed circuit boards are known in the art as disclosed by Dorfman. It is also true that Dorfman indicates "that other hardware configurations could be utilized". However, it is not even remotely true that Don provides another hardware configuration for the Dorfman computer telephony system. The Don patent teaches a method and apparatus for verifying organization of a magnetic disk storage system and contains no discussion whatever of hardware configurations. The discussion at column 4, lines 55-65 of Dorfman relates to different types of backplanes. The Don patent does not provide an alternate backplane configuration or an alternate hardware configuration of any type. A method and apparatus for verifying organization of a magnetic disk drive system does not provide an alternate hardware configuration for a computer telephony server. A person of skill in the art reviewing Dorfman would not consult Don for an alternate hardware configuration. Accordingly, the combination of Dorfman and Don is improper and does not establish a *prima facia* case of obviousness.

Assuming for the sake of argument that Dorfman and Don are properly combinable, the references, taken individually or in combination, do not teach or suggest a plurality of circuit boards each having electronic circuitry including a non-volatile memory containing product data that identifies the respective circuit board, as required by claim 1. As acknowledged by the Examiner, Dorfman contains no disclosure or suggestion whatever of providing on a circuit board a non-volatile memory containing product data. The Examiner correctly states that Dorfman discloses the use of a ROM (col. 4, line 22). However, the ROM is part of memory 54 and is not located on the circuit boards in the backplane. Further, Dorfman is completely silent as to storing in the ROM product data that identifies the circuit board. Don discloses the

concept of a unique signature, but the signature identifies a storage logical volume rather than a circuit board, as claimed. The ID data structure of the storage logical volumes is described by Don at column 4, lines 60-65; column 5, lines 11-24; column 5, lines 48-64; and column 6, lines 16-27. Although the ID data structure of Don may provide the physical location of the storage logical volume, Don contains no disclosure or suggestion of storing on a circuit board product data that identifies the respective circuit board and means for reading the product data. Don addresses the problem of data loss in a disk storage system by providing storage logical volumes with signatures. This is very different from storing on a circuit board product data that identifies the circuit board. For these reasons, claims 1-4 and 6 are patentably distinguished over Dorfman in view of Don.

2. The claims of Group II patentably distinguish over Dorfman in view of Don and Wilhelm.

Claim 5 patentably distinguishes over Dorfman in view of Don and Wilhelm because the cited references fail to disclose or suggest circuit boards further comprising means for providing external access to the product data in the non-volatile memory through the backplane, as required by claim 5. The Examiner cites Wilhelm as teaching a system where external access is provided via bus receptacles on the backplane. However, an externally accessible bus system is very different from means for providing external access to product data in a non-volatile memory, as claimed. For these reasons, and for the reasons discussed above in connection with claim 1, claim 5 is clearly patentable over Dorfman in view of Don and Wilhelm.

3. The claims of Group III patentably distinguish over Dorfman in view of Don.

For the claims of Group III, claim 7 is representative. Claim 7 is directed to a computer storage system comprising an array of storage devices, a system cache memory, and a plurality of controller boards for controlling data transfer to and between the array of storage devices, the system cache memory and a host computer. Each of the controller boards has

electronic circuitry including a non-volatile memory containing product data that identifies the respective controller board and means for reading the product data in the non-volatile memory.

As discussed above in connection with claim 1, the Examiner has failed to establish a *prima facia* case of obviousness. Accordingly, the combination of Dorfman and Don is improper and should be withdrawn.

Assuming for the sake of argument that the combination of Dorfman and Don is proper, the references, taken individually or in combination, do not disclose or suggest the limitations of claim 7. It is true that Don describes a magnetic disk storage system. However, neither cited reference discloses a computer storage system having a system cache memory and a plurality of controller boards for controlling data transfer to and between the array of storage devices, the system cache memory and a host computer. Furthermore, the combined teachings of the references do not disclose or suggest controller boards having electronic circuitry including a non-volatile memory containing product data that identifies the respective controller board and means for reading the product data in the non-volatile memory. As discussed above, Dorfman contains no teaching whatever regarding a memory containing product data. Don describes ID data structures which identify storage logical volumes. For these reasons and for the reasons discussed above in connection with claim 1, claims 7-9 and 11 patentably distinguish over Dorfman in view of Don.

4. The claims of Group IV patentably distinguish over Dorfman in view of Don and Wilhelm.

Claim 10 patentably distinguishes over Dorfman in view of Don and Wilhelm because the cited references fail to disclose or suggest a backplane for mounting and interconnecting the controller boards, wherein each of the controller boards further comprises means for providing external access to the product data in the non-volatile memory through the backplane, as required by claim 10. As discussed above in connection with claim 5, Wilhelm fails to disclose or suggest means for providing external access to product data in a non-volatile memory, as claimed. For these reasons and for the reasons discussed above in connection with claims 1, 5 and 7, claim 10 patentably distinguishes over Dorfman in view of Don and Wilhelm.

5. The claims of Group V patentably distinguish over Dorfman in view of Don.

For the claims of Group V, claim 12 is representative. Claim 12 is directed to a method for identifying a circuit board, comprising the steps of placing a non-volatile memory device on the circuit board, storing product data that identifies the circuit board in the non-volatile memory device and reading the product data in the non-volatile memory device.

Dorfman does not disclose or suggest storing product data that identifies a circuit board in a non-volatile memory device and does not disclose or suggest reading the product data in the non-volatile memory device. As discussed above, Don fails to disclose storing on a circuit board product data that identifies a circuit board in a non-volatile memory device, as claimed. Don describes the association of ID data structures with storage logical volumes. As further discussed above, the Examiner has not established a *prima facia* case of obviousness based on the alleged combination of Dorfman and Don. For these reasons and the reasons discussed above in connection with claims 1 and 7, claims 12-14 are patentably distinguished over Dorfman in view of Don.

Conclusion

For the foregoing reasons, claims 1-14 are clearly and patentably distinguished over the cited prior art. Accordingly, the Board is respectfully requested to reverse the final rejection.

Respectfully submitted,
Scaringella et al., Applicants

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Docket No. E0295.70126US00
Date: December 22, 2003
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IX. APPENDIX: CLAIMS INVOLVED IN THE APPEAL (37 CFR § 1.192(c)(9))

1. Apparatus comprising:

a plurality of circuit boards, each having electronic circuitry including a non-volatile memory containing product data that identifies the respective circuit board and means for reading the product data in said non-volatile memory; and

a backplane for mounting and interconnecting said circuit boards.

2. Apparatus as defined in claim 1 wherein said non-volatile memory comprises a read-only memory.

3. Apparatus as defined in claim 1 wherein said non-volatile memory comprises an electrically-erasable programmable read-only memory.

4. Apparatus as defined in claim 1 wherein said non-volatile memory comprises a serial EEPROM.

5. Apparatus as defined in claim 1 wherein said each of said circuit boards further comprises means for providing external access to the product data in said non-volatile memory through said backplane.

6. Apparatus as defined in claim 1 wherein said product data includes one or more of a board part number, a board serial number, a board revision level, a cabinet serial number and text comments.

7. A computer storage system comprising:

an array of storage devices;

a system cache memory; and

a plurality of controller boards for controlling data transfer to and between said array of storage devices, said system cache memory and a host computer, each of said controller boards having electronic circuitry including a non-volatile memory containing product data that identifies the respective controller board and means for reading the product data in said non-volatile memory.

8. A computer storage system as defined in claim 7 wherein said non-volatile memory comprises a read-only memory.

9. A computer storage system as defined in claim 7 wherein said non-volatile memory comprises a serial EEPROM.

10. A computer storage system as defined in claim 7 further comprising a backplane for mounting and interconnecting said controller boards, wherein each of said controller boards further comprises means for providing external access to the product data in said non-volatile memory through said backplane.

11. A computer storage system as defined in claim 7 wherein said product data includes one or more of a board part number, a board serial number, a board revision level, a cabinet serial number and text comments.

12. A method for identifying a circuit board, comprising the steps of:

placing a non-volatile memory device on the circuit board;

storing product data that identifies the circuit board in the non-volatile memory device; and

reading the product data in said non-volatile memory device.

13. A method as defined in claim 12 wherein the step of storing product data comprises storing one or more of a board part number, a board serial number, a board revision level, a cabinet serial number and text comments.

14. A method as defined in claim 12 wherein the non-volatile memory device comprises a serial EEPROM.